Short Papers

A 23.8-GHz SOI CMOS Tuned Amplifier

Brian A. Floyd, Leathen Shi, Yuan Taur, Isaac Lagnado, and Kenneth K. O

***Abstract*—A 23.8-GHz tuned amplifier is demonstrated in a partially scaled 0.1-μm silicon-on-insulator CMOS technology. The fully integrated three-stage amplifier employs a common-gate, source–follower, and cascode with on-chip spiral inductors and MOS capacitors. The gain is 7.3 dB, while input and output reflection coefficients are −45 and −9.4 dB, respectively. Positive gain is exhibited beyond 26 GHz. The amplifier draws 53 mA from a 1.5-V supply. The measured on-wafer noise figure is 10 dB, while the input-referred third-order intercept point is −7.8 dBm. The results demonstrate that 0.1-μm CMOS technology may be used for 20-GHz RF applications and suggest even higher operating frequencies and better performance for further scaled technologies.**

***Index Terms*—CMOS, K-band, low-noise amplifier, negative resistance, silicon-on-insulator, SOI, spiral inductor, tuned amplifier.**

I. Introduction

CMOS technologies are approaching the sub-tenth-micrometer regime. These technologies will provide cutoff frequencies above 100 GHz and 7–8 interconnect layers to accommodate on-chip passive components with acceptable quality factors. These trends point to CMOS being a viable option for RF applications at 18 GHz and above. Recent results that attest to this fact include a 0.18-μm distributed amplifier used as a 16.6-GHz oscillator [1], a 0.18-μm 23-GHz amplifier using a cascode and on-chip transmission lines for matching [2], and a 0.1-μm 25.9-GHz voltage-controlled oscillator [3]. From these, it can be seen that CMOS transistors can be used to implement circuits operating above 20 GHz.

To further investigate the RF potential of deep submicrometer CMOS technology including noise and linearity performance, a tuned amplifier, which operates at 23.8 GHz, has been implemented in a partially scaled 0.1-μm silicon-on-insulator (SOI) CMOS technology. The process uses a 0.35-μm design rule set for all dimensions, except for the 0.1-μm effective gate length (0.15-μm drawn gate length) and 3-nm gate oxide thickness. Two metal layers (0.7 μm each) are available in the process and the substrate resistivity is 1–2 $\Omega \cdot$ cm. Partially depleted floating-body SOI transistors are used for all circuitry and the NMOS transistor f_T is 95 GHz.

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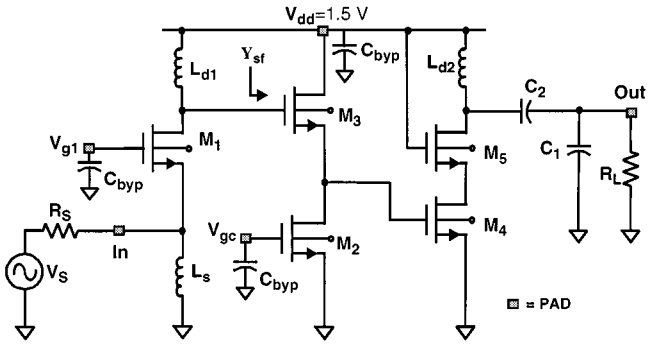

Fig. 1. Schematic of 0.1-μm 23.8-GHz SOI CMOS tuned amplifier.

II. Circuit Implementation

Fig. 1 shows a schematic of the fully integrated tuned amplifier. A three-stage topology was chosen to meet the targeted performance specification of 20 dB of gain at $\sim$ 18 GHz. Although a single-stage source-degenerated cascode topology matched to 50 Ω at the input and output would have resulted in reduced power consumption and a simpler design, such a stage typically provides at most 12–15 dB of gain in a CMOS technology [4]–[7]. Hence, multiple amplifier stages were required. For ease of input matching, a common-gate input stage with a shunt inductor is used. At resonance, the input impedance to the amplifier is $\sim 1/g_{m1}$. Therefore, g_{m1} is designed to be 0.02 Ω^{-1} to provide a 50-Ω power match. Following the input stage is a source–follower buffer, which then drives a common-source cascode stage with a tuned load. The output of this stage is matched to 50 Ω using a capacitive transformer.

The source–follower is used to shift the dc-bias level from the output of the first stage (at V_{dd}) to the input of the third stage. The bias point of the source–follower is controlled through input V_{gc}, which controls the current through M_2 and sets the V_{gs} of M_3. A source–follower with a capacitive load can have a negative input conductance. Referring to Fig. 1, it can be shown that the input admittance looking into M_3 is as follows:

$$\mathrm{Re}\,(Y_{\mathrm{sf}}) = G_{\mathrm{sf}} = \frac{\omega^2\left[g_T C_{gs3}^2 - g_{m3} C_{gs3} C_{LT}\right]}{(g_{m3}+g_T)^2 + \omega^2 (C_{gs3}+C_{LT})^2} \tag{1}$$

$$\mathrm{Im}\,(Y_{\mathrm{sf}}) = B_{\mathrm{sf}} = \frac{\omega C_{gs3}\left(g_{m3} g_T + g_T^2 + \omega^2\left(C_{gs3} C_{LT} + C_{LT}^2\right)\right)}{(g_{m3}+g_T)^2 + \omega^2 (C_{gs3}+C_{LT})^2} + \omega C_{gd3} \tag{2}$$

where g_T is the total output conductance at the source–follower output node (equal to $g_{ds3}+g_{ds2}$) and C_{LT} is the total capacitance at the same node (equal to $C_{gs4} + C_{sb3} + C_{db2} + C_{gd2}$). When $g_{m3} C_{gs3} C_{LT}$ is greater than $g_T C_{gs3}^2$, G_{sf} is negative. Negative conductance indicates that energy is being generated. When a source–follower is used after an amplifier containing an inductive load, this energy replenishes some of the energy lost in the inductor, causing the effective quality factor to increase. However, too much negative conductance can make the circuit unstable; thus, the conductance is adjusted such that the gain is improved while the stability is maintained.

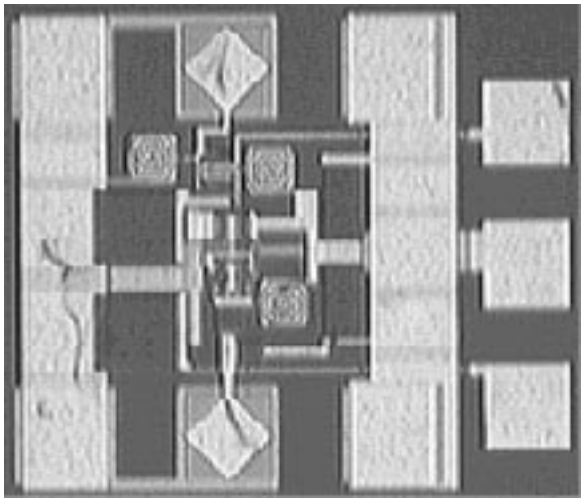

Fig. 2. Die photograph of 0.1-μm 23.8-GHz SOI CMOS tuned amplifier.

The S_{21} of the three-stage amplifier (when connected to 50-Ω transmission lines at the input and output) is approximately

$$\begin{aligned}|S_{21}| &= 2 \cdot |A_v|_{\omega=\omega_o} \\ &= 2\,|A_{v,cg} \cdot A_{v,\mathrm{sf}} \cdot A_{v,cs}| \\ &= 2 \cdot \left|\frac{g_{m1} Q_{Ld1}^{\mathrm{eff}} \omega_o L_{d1}}{1 + g_{m1} R_s}\right| \left|\frac{g_{m3} + j\omega C_{gs3}}{g_{m3} + g_T + j\omega\,(C_{gs3} + C_{LT})}\right| \\ &\quad \cdot \left|\frac{g_{m4} Q_{Ld2} \omega_o L_{d2}}{2n\,(\omega_0)}\right| \end{aligned} \tag{3}$$

where $n(\omega)$ is a complex capacitive transformer ratio as follows:

$$n(\omega) = \frac{1 + j\omega\,(C_1 + C_2)\,R_L}{j\omega C_2 R_L}. \tag{4}$$

An effective quality factor for L_{d1} accounting for the negative input conductance of the source–follower buffer is defined as

$$Q_{Ld}^{\mathrm{eff}} = \frac{Q_{Ld}}{1 - \Big(|G_{\mathrm{sf}}| \cdot Z_{Ld}\,(\omega_o)\Big)} \tag{5}$$

where Z_{Ld} is the resistance of the first stage tank at its resonance. This effective quality factor can be used whenever a tuned gain stage is followed by negative conductance (resistance) generator. The voltage gains for each stage, as simulated with SOISPICE [8], were 16, -4, and 3 dB for $A_{v,cg}$, $A_{v,\mathrm{sf}}$, and $A_{v,cs}$, respectively, showing that most of the gain was placed in the first stage. With the input impedance designed to be $R_S = 50\ \Omega$ (i.e., $g_{m1} = 0.02\ \Omega^{-1}$) and with $L_{d1} = L_{d2} = L_d$, the total forward transducer gain becomes

$$|S_{21}| = 2 \cdot |A_v|_{\omega=\omega_o} = \frac{1}{2}\frac{g_{m4}}{R_S} Q_{Ld1}^{\mathrm{eff}} Q_{Ld2} \omega_o^2 L_d^2 \left|\frac{A_{v,\mathrm{sf}}}{n\,(\omega_o)}\right| \tag{6}$$

where $A_{v,\mathrm{sf}}$ is the voltage gain through the source–follower, defined in (3).

Fig. 2 shows a die photograph of the SOI amplifier. The die size is 0.44×0.51 mm^2. Ground-shielded [9] diamond-shaped pads are used at the input and output to reduce the substrate resistance and capacitance. On-chip accumulation-mode MOS capacitors of 4.8 pF are used to bypass V_{dd}, V_{g1}, and V_{gc}. Three on-chip spiral inductors of 0.55 nH are used in the circuit. These inductors each occupy an area of 43×43 μm^2 and have 4.25 turns with a metal width and turn spacing of 3.8 and 1 μm, respectively. Metals 1 and 2 were shunted to decrease the series resistance. To design these inductors, Greenhouse's formula [10] was used for inductance calculation, while both the process data and inductors implemented and characterized in an earlier run of the 0.1-μm SOI technology at 15 GHz [11] were used to model the remaining inductor parasitics and calibrate the inductor model.

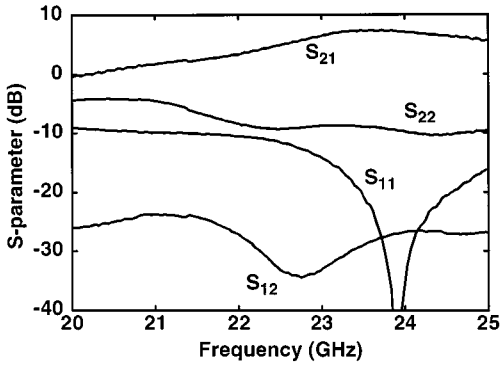

Fig. 3. Measured S-parameters of tuned amplifier.

III. Measured Results

The measured S-parameters of the 23.8-GHz SOI amplifier are shown in Fig. 3. These measurements were obtained on-wafer using GGB probes. At 23.8 GHz, the amplifier is perfectly matched at the input, with an S_{11} of -45 dB and well matched at the output, with an S_{22} of -9.4 dB. The transducer gain (S_{21}) is 7.3 dB, while the reverse isolation is 27 dB, which are both notable for a CMOS circuit at this frequency range. Also, the gain is greater than 0 dB beyond 26 GHz. The total supply current is 53 mA for a 1.5-V supply, which is high due to the use of multiple amplifier stages.

The measured quality factor (Q) of the on-chip spiral inductors is $\sim$ 2 at 24 GHz, while the inductance is $\sim$ 0.5 nH. These values were obtained by measuring an inductor test structure and an open pad structure and then subtracting the pad Y-parameters from that of the inductor with pads. The Q was calculated from the resultant Y-parameter data using the half-bandwidth method [12]. The Q is significantly lower than expected, which resulted in decreased gain, as will be discussed in Section IV.

Multistage amplifiers can exhibit poor linearity, and negative conductance can potentially affect this linearity even further. The measured $P_{1\mathrm{dB}}$ is -10 dBm (-16.2 dBm referred to the input), while the input-referred third-order intercept point (IIP3) is -7.8 dBm. These linearity data are considerably better than those obtained in [11], which is an encouraging result, indicating that acceptable linearity can be achieved with amplifiers utilizing source–followers.

Fig. 4 shows the measured noise figure (NF) and insertion gain (G_{ins}) versus frequency. The gain is 8.1 dB at 23.8 GHz, while the NF is 10 dB, which is very high. The high NF is caused by the reduced first-stage gain due to the low inductor Q. The noise associated with the input inductor L_S also increases NF. The low gain allows noise from stages 2 and 3 to refer to the input of the circuit. The 10-dB NF certainly is too high for typical wireless communication systems and can be decreased through circuit optimization and improving the inductor performance.

IV. Discussion

The measured results represent the highest operating frequency to date for a CMOS amplifier utilizing on-chip passive components. However, the measured gain was significantly lower than expected, which also led to increased NF. Circuit simulations performed using SOISPICE predicted an S_{21} of 21 dB, a tuned frequency of 18.7 GHz, an S_{11} and S_{22} of -17 and -5 dB, respectively, and an S_{12} of -32 dB. The simulated S-parameters are shown in Fig. 5. The relative

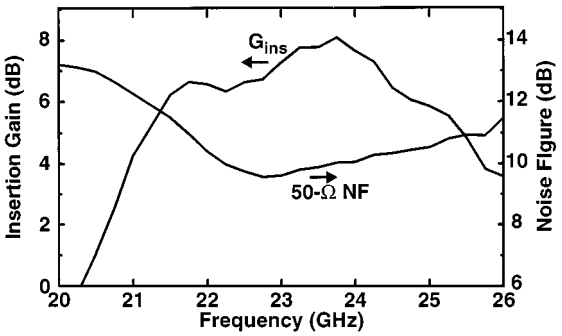

Fig. 4. Measured 50-Ω NF and insertion gain ($G_{\rm ins}$) versus frequency.

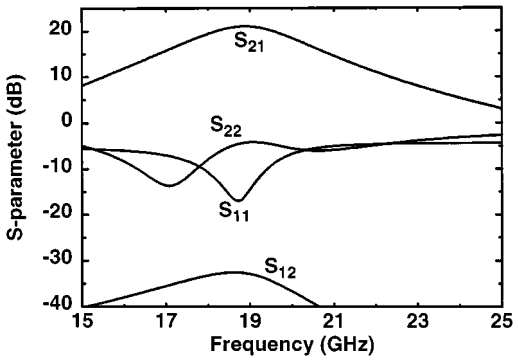

Fig. 5. Simulated S-parameters of a tuned amplifier.

accuracy of the SOISPICE transistor models used in the simulation was demonstrated through the implementation of a dynamic SOI CMOS frequency divider on the same die that had a simulated upper frequency limit of 18 GHz, while the measured limit was 18.75 GHz [13]. Therefore, the difference between simulated and measured gain is primarily attributed to low inductor Q. The inductor Q's used in the simulations were 4.8, obtained using the half-bandwidth method Q-extraction technique [12] on the designed inductor model. Using simulated values for all quantities, except those involving the inductor in (6), and inserting $Q_{Ld} = 2$ and $L_d = 0.5$ nH results in an S_{21} of 7.5 dB, accounting for the 13.7-dB degradation in gain. The 10% reduction in inductance also results in a 1-GHz increase in resonant frequency. The remaining frequency shift is attributed to overly pessimistic modeling of interconnect capacitance and slightly decreased transistor parasitic capacitance.

Clearly, the inductor Q should be improved. Natural improvement to the inductor Q will come by using a 0.1-μm CMOS technology with a fully developed back end (i.e., six or more metal layers). This would result in increased top-level metal thickness—decreasing series resistance—and increased distance between the top-level metal and the substrate—reducing parasitic capacitance and the impact of substrate resistance on Q. Also, using copper rather than aluminum for the metal will further enhance the inductor Q. Given the two-layer back end currently used and the 1–2-$\Omega \cdot$ cm substrate resistivity, the inductor Q could be improved by using a patterned ground shield [14] to terminate the electric field before it reaches the substrate. The patterned ground shield would reduce the substrate resistance at the cost of decreased self-resonant frequency. All of these improvements together have been used to implement ground-shielded 0.7-nH spiral inductors with Q's of 20 at 20 GHz in a 0.18-μm technology with copper interconnects and a 15–25-$\Omega \cdot$ cm substrate resistivity [15], [16].

Finally, simulations with the updated inductor models were used to examine the efficacy of the source–follower buffer. The simulated input conductance to the source–follower is -2 mS, resulting in a $Q^{\rm eff}$ of 2.8.

TABLE I
PERFORMANCE SUMMARY FOR 23.8-GHz SOI TUNED AMPLIFIER

Parameter	Result	Parameter	Result
Resonant Frequency	23. 8 GHz	NF	10 dB
S_{21}	7.3 dB	P_{1dB}(in)	-16.2 dBm
S_{11}	-45 dB	IIP3	-7.8 dBm
S_{22}	-9.4 dB	V_{dd}	1.5 V
S_{12}	-27 dB	Supply Current	53 mA

Therefore, the negative conductance of the source–follower improves S_{21} by a factor of ~ 1.4. However, the voltage gain through the buffer ($|A_{v,\rm sf}|$) is ~ 0.63. Therefore, the net gain in S_{21} due to the source–follower is $1.4 * 0.63 \cong 0.9$. Thus, for this amplifier and bias condition, while the source–follower is providing a needed dc level shift between stages 1 and 3, the gain is slightly reduced. A potential better use for the source–follower would be to use it purely as a negative conductance generator in parallel with the inductor, without passing a signal through the stage. In such an implementation, the first common-gate stage could be coupled to the third common-source cascode stage through a capacitor, having the additional benefit of separating the bias conditions of the source–follower buffer and the common-source cascode.

V. CONCLUSIONS

This paper has presented a 23.8-GHz 7.3-dB multistage tuned amplifier, providing an early look at what may be possible in sub-tenth-micrometer CMOS technologies. This circuit has the highest operating frequency to date for a CMOS amplifier utilizing on-chip passive components. A summary of the results is shown in Table I. While only moderate noise and linearity performance are obtained, once a fully scaled CMOS technology with a more advanced back-end process is used, the results should dramatically improve. These improvements will be due to increased inductor Q, decreased parasitic capacitance, which allows the inductance, and, hence, gain to increase and further circuit optimization. Finally, these results show that a 0.1-μm CMOS technology should be able support RF applications above 20 GHz and suggest even higher operating frequencies for further scaled CMOS technologies.

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Effect of Conductive Perturber Diameter on Nonresonant Measurement of Interaction Impedance for Helical Slow-Wave Structures

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***Abstract*—The measurement accuracy of the interaction impedance for a helical slow-wave structure (SWS) using the nonresonant perturbation method has been studied using conductive wire perturbers with different diameters. Data obtained by the measurement were compared with a rigorous numerical analysis. It is shown that the measured values of the interaction impedance for the helical SWS converge to those obtained by using a three-dimensional finite-element computational method when the diameter of the perturber is reduced to less than 10% of the helix diameter.**

***Index Terms*—Helical slow-wave structure, interaction impedance, nonresonant perturbation measurement, traveling-wave tube.**

I. Introduction

An accurate estimation of interaction impedance, which is correlated with gain and efficiency of a device such as a traveling-wave tube (TWT), is an important step for the design of the device. On-axis interaction impedance was defined by Pierce [1] as

$$K = \frac{E_z^2}{2\beta_0^2 P} \tag{1}$$

where E_z is the longitudinal component of fundamental space harmonic amplitude of an on-axis electric field, β_0 is the propagation constant of this harmonic in the absence of an electron beam, and P is the total power flow through a interaction structure.

The measurement method commonly used for this purpose [2] employs a finite-size dielectric or conductive rod inserted into the structure as a perturber. The measurement indicates the relative electric-field strength through the change in the propagation constant of the structure. A large portion of a systematic error of the conventional perturbation theory, upon which this method is based, is attributed to the omission of the effects produced by space harmonics and TE fields [3]. The effects of the space harmonics were theoretically taken into consideration by several researchers [4], [5].

In this paper, a very thin (hairline) conductive wire is employed to minimize the effects of the space harmonics and TE fields on the interaction impedance measurement. The hairline conductive wire can be placed much closer to the helix axis where the uniform longitudinal field dominates and the effects of the space harmonics and TE fields can be fairly reduced.

This paper aims at investigating the effect of the conductive wire diameter on the measurement accuracy of the interaction impedance in order to evaluate an adequacy and limitation of such a nonresonant measurement method. The study is based on comparison of the measured data with that is obtained by a three-dimensional (3-D) finite-element numerical simulation with an automatic adaptive mesh optimization. This simulation code, i.e., HFSS [6], applies a quasi-periodic boundary condition to the helical slow-wave structure (SWS), where the phase shift per period along the axial distance is specified at the ends of the structure. The phase velocity of the helical SWS is obtained using the eigenmode solution method, where frequency versus phase shift characteristics are found by calculating the eigenfrequencies of the truncated structure satisfying the boundary condition specified. The interaction impedance of the helical SWS is obtained by directly computing E_z and P in the HFSS code.

From the nonresonant perturbation measurement, the on-axis interaction impedance for the helical SWS was derived as [7]

$$K = \frac{120}{k}\frac{\Delta\beta}{\gamma\rho}\frac{\gamma_0^2}{\beta_0^2}\frac{1}{I_0(\gamma_0\rho)\left[I_1(\gamma\rho) + \dfrac{I_1(\gamma\rho)}{K_0(\gamma\rho)}K_1(\gamma\rho)\right]} \tag{2}$$

where β_0 and γ_0 are the axial and radial propagation constants of the unperturbed structure, respectively. γ is the radial propagation constant of the perturbed structure and $\Delta\beta$ is the change in propagation constant between the unperturbed and perturbed structure. k is the propagation constant in free space. I_0 and K_0 are the first and second modified Bessel functions. ρ is the radius of a conductive wire. Equation (2) is derived using the nonresonant perturbation theory and scattering model of the secondary perturbed field due to the insertion of a thin conductive wire. A small perturbation is assumed to take an advantage of the very thin conductive wire. It is important that the space harmonic effect becomes negligible for a sufficiently thin conductive wire.

As shown theoretically in [7], the errors of (2) caused by other assumptions of the perturbation theory depend on the wire diameter and frequency. The accuracy verification of (2) is carried out over a 1.5-octave frequency range with a variation of a wire diameter from 2% to 30% of a helix diameter.

II. Experiment

The change in propagation constant $\Delta\beta$ and the propagation constant β_0 is measured experimentally. Fig. 1 shows the measurement

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